Rapid Tag Collision Resolution Using Enhanced Continuous Wave Absence Detection

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***Abstract*—In RFID tag identification, tag-to-tag collisions pose a challenging problem to protocol designers. Currently the modulation silencing mechanism (MSM) has been proposed to overcome the time and power wasted on collision slots during tag identification. In MSM, the time of collision slots is reduced by the assistance of the continuous wave absence detection (CWAD) circuit. CWAD allows the tags to sense the reader's RF signal cutoff and terminate data modulation. In this paper, we propose an enhanced CWAD (ECWAD) design to reduce the time required for RF cutoff detection. The ECWAD circuit mitigates the tag-to-tag collision effects on both identification efficiency and throughput. ECWAD is a fast and low power sensing circuit that allows having shorter collision slots, faster tag identification, and limited voltage drop at the tag. When compared to the existing CWAD design, the proposed design detects the RF signal cutoff by the reader in less than 20% of that in CWAD and reduces the collision slot time by more than 32%.**

I. Introduction

Radio Frequency IDentification (RFID) systems facilitate cost effective automatic data collection in several applications (e.g., supply chain management, pharmaceutical industry and airports). In such applications, mobile or fixed RFID readers collect the unique identification (ID) from the tags (which are attached to the targeted objects) and report the collected data to a central host. Therefore, time and power efficient identification protocols are crucial in enabling prompt tag identification by fixed readers and to extend the battery life of mobile readers.

A passive RFID tag is a battery-less integrated circuit with a radio frequency (RF) antenna that enables both tag communication with the reader and energy harvesting of the reader's signal to power up the tag's integrated circuit. Due to the limited power of passive tags, tag-to-tag inter-communication capabilities are unfeasible [1]. Consequently, RFID tags are incapable of organizing their data transmissions to the reader which makes simultaneous transmissions (also known as collisions) inevitable. To overcome this issue, probabilistic (ALOHA-based) [2] or deterministic (Tree-based) [3] time slotted anti-collision protocols are executed by readers to reduce the *number* of simultaneous transmissions. Unfortunately, even at optimal settings of such protocols, collisions slots to the total slots is 26% in probabilistic protocols [4] and 50% in deterministic protocols [3].

Modulation Silencing Mechanism (MSM) [5] has been proposed as a *time* reduction mechanism of collision slots. MSM is applicable to the existing time slotted protocols in order to achieve a reduction in both *number* and *time* of the collision slots. MSM is based on the coordination between the reader and the collided tags to end collision slots. During collision slots, the reader terminates its continuous wave (CW) and the replying tag(s) senses this termination by the continuous wave absence detection (CWAD) circuit. CWAD triggers the tags to stop data modulating if the reader's CW termination exceeds a predefined time interval. The CWAD circuit presented in [5] did not consider the rectifier's effect on prolonging the detection time. In addition, to trigger modulation silencing in the collided tags, CWAD output should drop to a low voltage that pulls down the voltage of the tag's IC and may cause the tag to reset its status registers.

In this paper, we propose an enhanced CWAD (ECWAD) design that provides a prompt CW cutoff detection regardless of the capacitance of the tag's rectifier. The ECWAD is based on the voltage comparison of two low power resistor-capacitor (RC) cells to trigger modulation silencing in the tag. The proposed circuit is evaluated based on the timing of the EPC Class 1 Gen 2 standard. When compared with the design in [5], the proposed design consumes less energy and reduces the detection time to less than 20%. This results in shorter collision slots and hence, shorter tags identification time by 30% in dense tag population environments.

The remainder of this paper is organized as follows. In Section II we discuss the related work. We propose our ECWAD design in Section III and evaluate its significance on existing RFID protocols in Section IV. The paper is concluded in Section V.

II. MSM and CWAD overview

A. MSM

MSM is a reader-tag interaction mechanism that enables the simple passive tags to decode a "stop command from the reader over a half-duplex backscattering channel. MSM components at the reader and the tag are depicted in Figure 1. At the reader, the reader execute rapid collision detection (RCD) algorithm that stops CW transmission upon the reception of an erroneous data from the tags. At the tag, a low complexity

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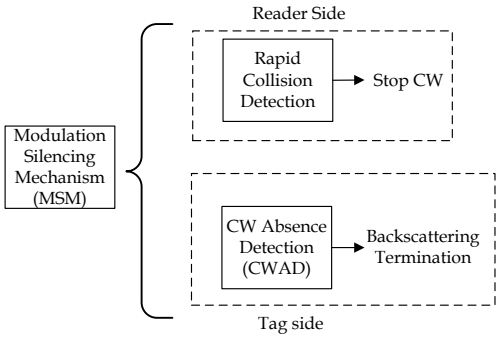

Fig. 1. MSM components

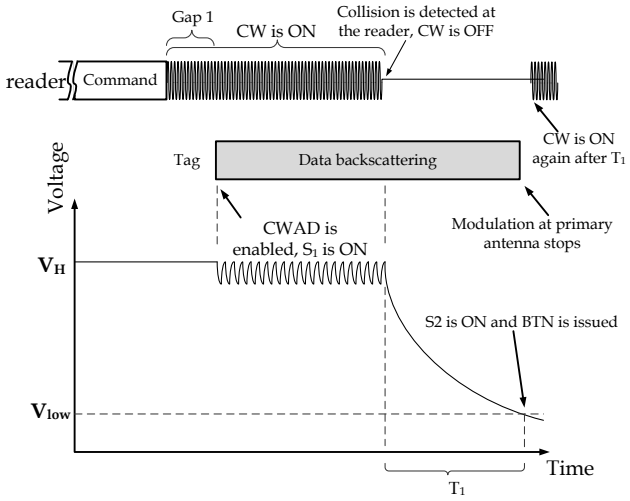

Fig. 2. Timing example of an collision detection during tag backscattering

circuit, Continuous Wave Absence Detection (CWAD), senses the reader's CW availability at the tag's antenna. If the CW is absent for a predefined period, noted as "T_1, the tag stops its data modulation.

A timing example of MSM interaction between the reader and the tag is shown in Fig. 2 to illustrate MSM operation. In every time slot, the reader sends a command and starts emitting a CW from its transmitter and filtering its reflection (from the tags) at its receiver. The addressed tag enables its CWAD circuit and starts modulating the load of its antenna to reflect/absorb (i.e., backscatter) the readers CW. In the example of Figure 2, at some point in the tag reply, the reader detects an erroneous transmission (e.g., corrupted data due more than one tag reply). Therefore, it stops CW transmission for a predefined time interval (T_1). The tag is designed to sense the absence of CW and stop modulating the load at its antenna within T_1. Note that the tag keeps modulating its load until it detects CW absence.

B. Continuous Wave Absence Detection (CWAD)

The CWAD circuitry is on the tag's side (as depicted in Fig. 1). CWAD is designed to interrupt the CW cutoff by the reader as a stop signal for the ongoing data backscattering by the tag. In [5], the CWAD circuit is designed for dual antenna tags and placed after the one of the rectifiers to prevent the CWAD from draining the voltage of the main capacitor as will be described shortly. In Fig.3, a block diagram of a dual antenna passive tag with the CWAD circuit is shown. The two antennas are attached to two independent charge pump rectifiers. The output of the rectifiers is stored in the main capacitor to power up the tags IC components (logic gates, memory, RF modulator, etc.). When the tag is not backscattering its data, the CWAD circuit is disabled, and the two rectifiers will be charging the main capacitor. If the tag is addressed by the readers command, the CWAD circuit is enabled and powered by the second rectifier.

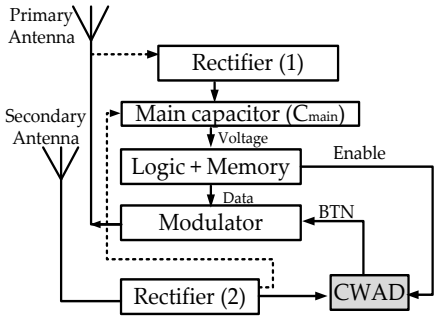

Fig. 3. Dual antenna tag main components with CWAD

The main components of the CWAD circuit are illustrated in Fig. 4. The capacitor C_{CWAD} is connected to the output of the rectifier. When the CWAD is enabled, the rectifier builds up the voltage from the CW and store it in C_{CWAD} instead of C_{main}. Since the output voltage of the rectifier depends on the tag's distance from the reader, a voltage limiter (sequence of diode-connected transistors) is placed parallel to C_{CWAD} to ensure a constant voltage from the rectifier. C_{CWAD} is also in parallel with both a pull down resistor R_{CWAD} and an active-low switch S_1 (e.g., a PMOS transistor). Once S_1 is "ON", C_{CWAD} discharges its voltage in R_{CWAD}. When the voltage across C_{CWAD} is low enough to turn the active-low switch S_2, the backscattering termination (BT) signal is asserted. Since the voltage over the capacitor should drop to a low voltage to assert the BT signal, it affects the voltage of the main capacitor if it attached to the same rectifiers. That was the motivation behind placing the CWAD in dual tag antennas.

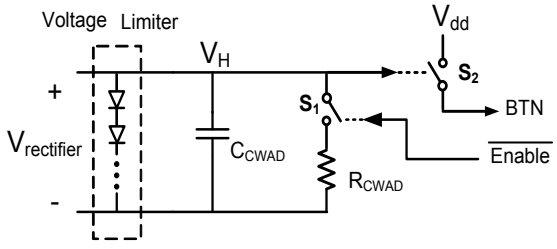

Fig. 4. CWAD circuit schematic showing the basic components [5]

The current design of CWAD has the following limitations:

- The design of the CWAD in Fig. 4 requires the voltage of the capacitor to drop to a level that is low enough to turn on an active low switch which drains the voltage at the main capacitor.
- Since the CWAD circuit is designed for dual antenna tags, it's wide adoption is limited as the dominant type of RFID tags are with single antenna.
- When the output voltage is high from the rectifier (e.g., when the tag is close to the reader), the voltage limiter in Fig. 4 drains any excess power and waste it through the diodes to the ground instead of storing it in the main capacitor.
- Due to the different input power at the tag's antenna, CWAD does not have a constant voltage level at the capacitor C_{CWAD} (i.e., it varies by distance). This causes a variance in the detection time that may exceed T_1.
- The existing CWAD design does not consider the effect of the capacitance of the rectifier on the cutoff detection delay which contribute to a substantial on CW absence detection time.

In the proposed design, we enhance the previous design to overcome the above shortcomings to provide fast and efficient CW cutoff detection.

III. Enhanced CWAD (ECWAD)

enhanced CWAD (ECWAD) is designed to replace the CWAD circuit in the tag side of the MSM in many applications that span tag identification [5], counting and estimation [6], and authentication [7]. A block diagram of the basic components of a single antenna passive tags is depicted in Fig. 5. In this diagram a low complexity circuit, ECWAD, is added to single antenna RFID tag in order to facilitate MSM. In this section ECWAD design, timing, and operational analysis are presented.

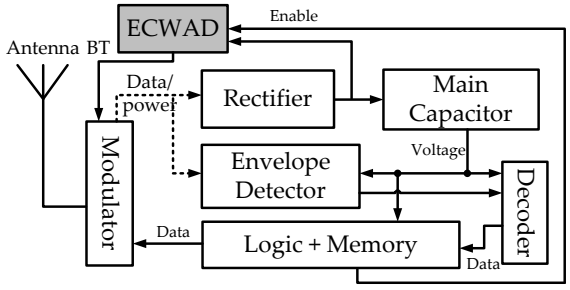

Fig. 5. Main Components of passive RFID tag with ECWAD circuit at the rectifier output.

A. ECWAD design

The tag's rectifier and the ECWAD circuit are illustrated in Fig. 6-a and 6-b, respectively. ECWAD consists of two RC cells and is placed after the rectifier to sense the CW signal. The first RC cell in Fig. 6-b provides an envelope detection of the output voltage from the rectifier, noted as V_H. The second RC cell provide the average voltage of the rectifiers output,

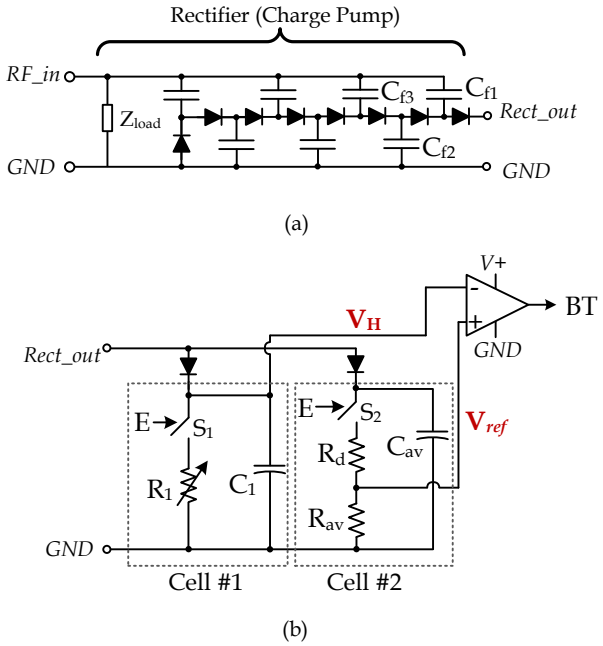

Fig. 6. A voltage rectifier and ECWAD circuit schematic showing its basic components. Z_{IC} is the IC's impdance. The rectifier's output is denoted as $Rect\_out$.

noted as V_{ref}. The envelope detector capacitor C_1 is smaller than the averaging capacitor C_{av}. The pull down resistor of the envelop detector cell (R_1) is also smaller than the combined resistors in the averaging cell ($R_d + R_{av}$). The pull-down resistors are activated by two active high switches S_1 and S_2. The two RC cells in Fig. 6 are isolated by two diodes to allow independent discharging as will be discussed shortly. R_d and R_{av} are used to divide the voltage across C_{av}. The cells output V_H and V_{ref} are compared by a voltage comparator that is triggered to assert the backscattering termination signal V_H is lower than V_{ref} by a voltage difference threshold V_{diff}.

B. ECWAD operation

When tags are powered up, the voltages across C_1 and $C_{av}$are equal to the rectifier's output voltage. A waveform example is given in Fig. 7 to illustrate ECWAD operation.

The reader starts the slot by sending a command followed by CW transmission. After receiving the reader's command, all tags enable their ECWAD circuit by asserting the enable signal (E) to turn "*ON*" the switches S_1 and S_2. The addressed tag(s) by the reader command start backscattering the preamble followed by their data. Since the voltage at C_{av} is the same as C_1 (i.e., equals to V_H), V_{ref} is less than V_H by the drop at R_d when CWAD is activated as depicted in Fig. 7. Closing the switches S_1 and S_2 allows C_1 and C_{av} to discharge their voltage in R_1 and (R_d+R_{av}), respectively. At the same time, C_1 and C_{av} are charging from the output of the rectifier as long as CW is still "*ON*". The charging (from rectifier) and discharging (in the resistors) of the capacitors causes voltage rippling in V_H and V_{ref}.

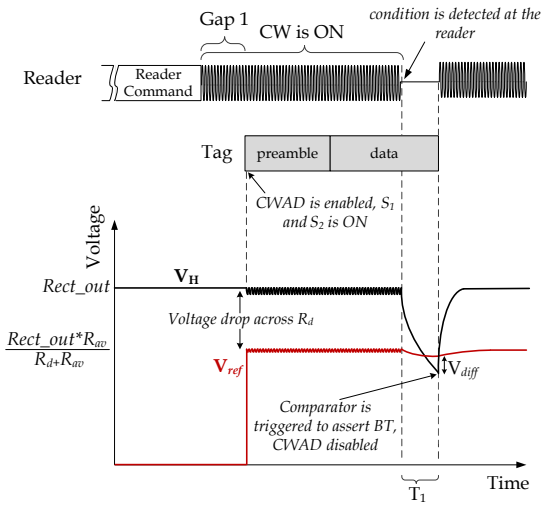

Fig. 7. Illustrative example of the voltage across C_1 and R_{av}.

In the example shown in Fig. 7, at some point during data backscattering, the reader detects a collision and stops its CW transmission for T_1. With no power at the tag antenna, the smaller capacitor C_1 discharges its voltage in R_1 at a higher rate than the larger C_{av} in (R_d+R_{av}). To detect CW cutoff, once the voltage V_H is less than V_{ref} -V_{diff}, the comparator is triggered to issue the backscattering termination (BT) signal.

C. ECWAD timing

The symbol duration from the tag to the reader (denoted as T_{pri} in the EPC standard) is set by the reader during communication initialization. The value of R_1 in ECWAD is changed to accommodate the different tag symbol duration. In tags that use AM to backscatter their symbols, the HIGH period of the symbols is backscattered by lowering the impedance at the antenna so that the CW is fully backscattered and no power is absorbed by the tag [8][1]. Therefore, during the HIGH period, the rectifier will not be charging the ECWAD capacitors. This might be mistaken as a CW cutoff if T_1 is shorter than the HIGH period duration of the tag's symbol. Therefore, to ensure that T_1 is always longer than the symbol's HIGH duration, R_1 is switched to larger values in longer T_{pri} durations and vice versa. T_1 is selected to be, at least, twice the HIGH period in tag's symbols. In the EPC standard, the HIGH period (T_{pri}/ 2) can be as low as 0.78μs and as high as 12.5μs [9]. Nonetheless, T_1 should be short to increase time saving, and to prevent the voltage at the main capacitor from dropping and resetting the tag. Table I lists some possible values for the components of ECWAD circuit that ensure T_{pri}<T_1< 2T_{pri}.

1) Rectifier capacitance effect: In order to have a proper operation of ECWAD, the time required by V_H to trigger the comparator has to be designed to be less than T_1. V_H starts

TABLE I
AN EXAMPLE OF ECWAD COMPONENTS VALUES THAT ENSURE T_{pri}<T_1< 2T_{pri} OF EPC STANDARD

Component	smallest $T_{pri}/2$ (0.78μs)	largest $T_{pri}/2$ (12.5μs)
R_1	**3MΩ**	**51MΩ**
R_{av}	45MΩ	45MΩ
R_d	5MΩ	5MΩ
C_1	5pf	5pf
C_{av}	70pf	70pf
V_{diff}	50mV	50mV

falling from V_{MAX} = $2N(V_{in} - V_{th})$ [2] with a time constant τ=R_1C_1; however, this is not the only time constant that controls the drop of V_H . A drop of (V_{in}-V_{th}) in V_H turns "ON" the diode touching C_1 by the higher voltage at the capacitor C_{f1} in the last stage of the rectifier of Fig. 6 (C_{f1} in parallel with C_1 will be discharging in R_1). Another drop of (V_{in}-V_{th}) at R_1 allows C_{f2} to start discharging, and so on. Fig. 8 presents a simulation of CWAD operation and the effect of the rectifier's capacitors on T_1.

The voltage V_H is dropping at a variable rates due to the increased capacitance at every drop of $(V_{in}-V_{th})$. The voltage drop for the first three time constants is expressed in euqation 1.

where $\tau_1 is R_1 C_c$, $\tau_2 is R_1 (C_c+C_{f1})$, and $\tau_3 is R_1 (C_c+C_{f1}+C_{f2})$. The three points in the Eq. (3.1) are presented in the waveforms of Figure 8.

The voltage V_{ref} is affected by a single time constant $\tau(V_{ref})$ =(R_{av}+R_2)C_{av}. Hence, to determine T_1, the time at which V_H drops below V_{ref} -V_{diff} depends on the following parameters:

- The voltage divider ratio between R_d and R_{av}.
- Comparator sensitivity V_{diff}.
- R_1, R_d, R_{av}, C_1, C_{av}, and the charge pump capacitors.
- The input voltage at the rectifier V_{in}
- The diodes threshold voltage V_{th}

By considering all the parameters that can affect the duration of T_1, a fast and precise set of T_1 values can be accommodated for each value of T_{pri}. For instance (by referring to Fig. 8), to eliminate the effect of the rectifier capacitors, V_{ref} can be designed to be very close to $V(C_{av})$ by making R_d<<R_{av}. This allows V_H to drop below V_{ref} - V_{diff} within the period t_1 which is controlled by C_1 only.

All the above parameters are controllable but the input voltage at the rectifier as it is a function of the input power at the antenna. The peak voltage of V_{in} is expressed as $\sqrt{2 * Z_{load} * 10^{P_{in}/10}}$, where P_{in} is the input power in dB. Nonetheless, the input power is an "uncontrollable" factor that can vary from one tag to another based on several factors (e.g., the distance between the reader and the tag and tag orientation). Different power levels cause different V_{in} at the tags. In Fig. 9 CWAD circuit is simulated with two different

[1]Tags that use Phase Modulation (PM) for backscattering harvest power in LOW and HIGH periods of the backscattered symbols, hence no lower limit of T_1 is required.

[2]where N is the number of stages in the charge pump rectifier, V_{in} is the input peak voltage at the tag antenna and V_{th} is the threshold voltage of the diodes in the rectifier.

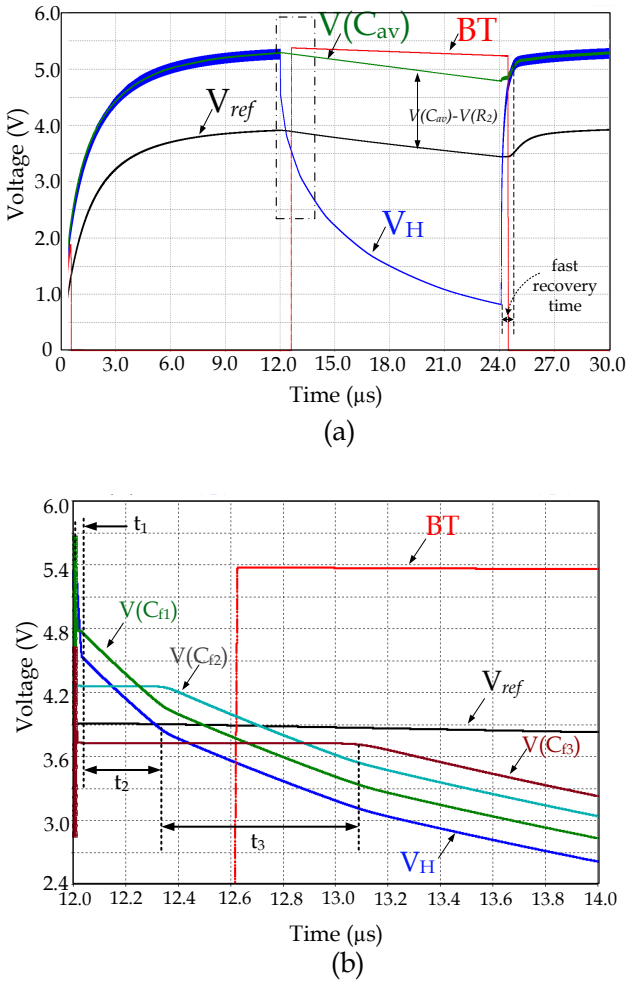

Fig. 8. Simulation of ECWAD and the effect of the rectifiers capacitors on the detection time T_1

input powers in PSPICE. CW cutoff occurs at the same time (2μs) for both input powers. While dropping, V_H reaches time points t_1, t_2, and t_3 of Equation(1) at different times for different input voltages. Accordingly, BT signal is triggered at different times. Therefore, to provide a reliable and consistent CW sensing within the first time constant τ_1, we reduce resistor R_d to be much less than R_{av} so that the small voltage drop over R_d keeps V_{ref} very close to V_H.

IV. Performance Evaluation

A. Simulation setup

To evaluate the time saving of ECWAD over CWAD we considered the *data-fields* and *timing* of the EPC standard specifications [9] in our simulations. The standard's message length consists of 128 bits for the Data field in the single slots (32 bits for protocol control (PC) and 96 bits for tag's unique ID) and 16 bits for CRC field (144-bits in total).

To determine the actual time duration of collision slot, the timing of each field in the slot is required. Based on the standards [9], [10], the key *timing* parameters that determine the slot length are:

- Tag to reader symbol duration, T_{pri}, which is a function of both encoding method and the Divide Ratio (DR).
- Reader to tag symbol duration (T_{ari}).

The reader is capable of setting different values for the *timing* parameters during the initialization phase of the identification. For instance, in [9], T_{ari} can range from 6.25μs up to 25μs. By considering the upper and lower bounds of T_{ari} and the different values of T_{pri}, the set of the possible combinations are presented in Table II. Note that T_{pri} is dependent on both encoding methods and DR. The different combinations of the above parameters result in different possible slot lengths of the collision slots, and consequently, different reduction ratios.

TABLE II
Possible slot parameter combinations

Timing Setting #	Encoding	T_{ari} (μs)	Divide Ratio
1	MM2	6.25	8
2	MM2	6.25	64/3
3	MM2	25	8
4	MM2	25	64/3

B. Detection power consumption

At a rectifier output of one volt, the power consumption of ECWAD for the smallest and largest possible T_{pri} is 353nW and 39nW, respectively. These values are a fraction of the IC power consumption [8], [11] and is only consumed when CWAD is "ON". At the same voltage, CWAD's total energy consumption for the same rectifier design is much higher than ECWAD. Note that in Fig. 8-a, if CWAD is employed, the time required to trigger the active low switch is when V_H is less than one volt, this indicates that the RC cell will keep draining the current into the ground (GND) for a substantial amount of time, that is more than 10 times the time required by ECWAD.

C. Collision slot time reduction

The collision slot structure is presented in Fig. 10. The difference between CWAD and ECWAD is in the detection time T_1. ECWAD is capable of detecting CW cutoff within $2*T_{pri}$ while CWAD requires $10*T_{pri}$ for detection (assuming that the rectifier capacitance did not prolong the CWAD operation). More than 80% of the detection time is saved by ECWAD which is reflected in shorter collision slots. The time saving in the collision slots based on the four timing settings in Table II is presented in Table III. In Table III, the total reduction in collision slots ranges from 18% up to 32% which translates a significant time saving especially when collisions are dominant (e.g., when large number of tags are to be identified).

D. Time efficiency of Anti-collision protocols

In our simulations, we compare CWAD and ECWAD by running Dynamic Framed Slotted ALOHA protocol with a

$$V_H = \begin{cases} V_{max} e^{t/\tau_1}, & \text{if } 0 < t < -\tau_1 \ln\left(\frac{V_{max}-V_{in}+V_{th}}{V_{max}}\right) = t_1 \ . \\ (V_{max} - V_{in} + V_{th})\, e^{t/\tau_2}, & \text{if } t_1 < t < -\tau_2 \ln\left(\frac{V_{max}-2V_{in}+2V_{th}}{V_{max}-V_{in}+V_{th}}\right) = t_2 \ . \\ (V_{max} - 2V_{in} + 2V_{th})\, e^{t/\tau_3}, & \text{if } t_2 < t < -\tau_3 \ln\left(\frac{V_{max}-3V_{in}+3V_{th}}{V_{max}-2V_{in}+2V_{th}}\right) = t_3 \ . \end{cases} \quad (1)$$

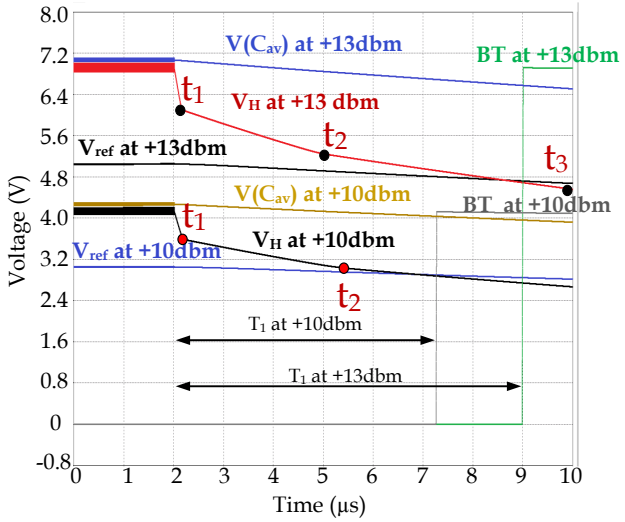

Fig. 9. Input power effect on the changing of CW cutoff detection time (T_1)

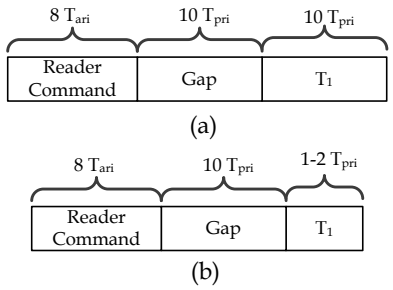

Fig. 10. Collision slots with (a) CWAD and (b) ECWAD, Gap is the time for command processing at the tag

maximum frame size of 512 slots [12], [13]. DFSA is selected for evaluation for its efficiency in managing large number of tags and for its use in the standards [9], [10]. The Tag populations are selected from the set P={10,20,30, ..., 4000}. Every population in P is identified 25 times and the average identification time is reported in the plots of Fig. 11 to Fig. 14.

TABLE III
COLLISION LENGTH IN CWAD ANF ECWAD

Timing Setting #	CWAD (μs)	ECWAD (μs)	reduction percentage
1	217	146	32%
2	145	118	18%
3	831	550	33%
4	542	436	19%

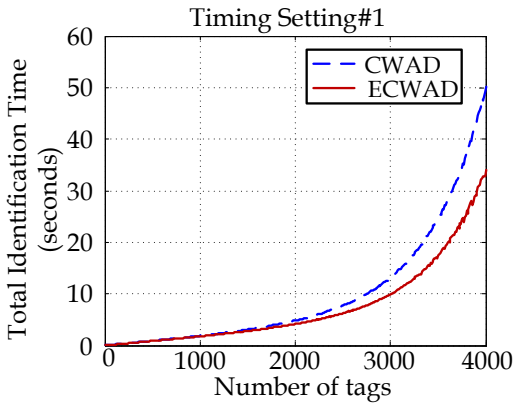

Fig. 11. Total identification time for tags with CWAD and ECWAD under timing setting#1 in Table II.

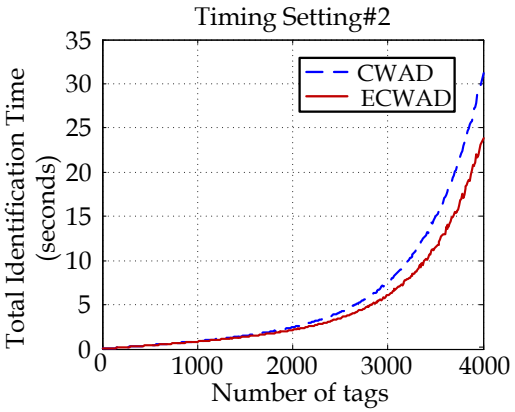

Fig. 12. Total identification time for tags with CWAD and ECWAD under timing setting#2 in Table II.

Note that the total identification time for tags with ECWAD is less than CWAD, especially in densely populated environments (i.e., over 1000 tags). The performances of DFSA in the above figures vary based on the different possible tag-to-reader bit length (T_{pri}) and the reader-to-tag bit length (T_{ari}) combinations.

Within the results of each setting, at low tag population, the performance of DFSA with N_{max} =512 slots shows almost the same total identification time. At higher tag population, collision slots start to contribute more when the frame size is smaller than tag population. Hence, the performance starts to drop faster (i.e., longer identification time) in CWAD than ECWAD as ECWAD facilitates shorter collision slots.

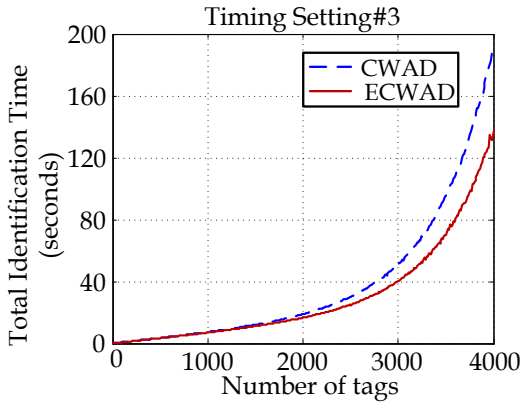

Fig. 13. Total identification time for tags with CWAD and ECWAD under timing setting#3 in Table II.

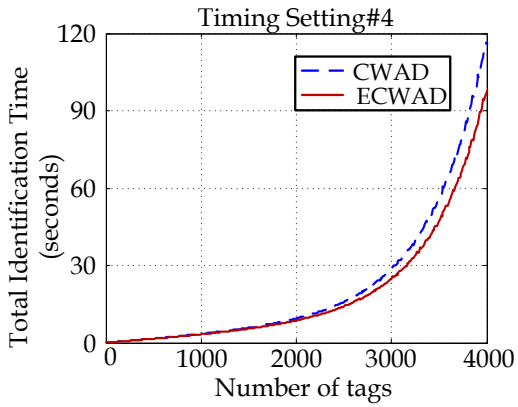

Fig. 14. Total identification time for tags with CWAD and ECWAD under timing setting#4 in Table II.

V. Conclusion

In this paper, we proposed an enhanced continuous wave absence detection (ECWAD) circuit at the tag that allows prompt and low power detection of the reader's CW cutoff. The efficient circuit enables faster collision slot termination and hence, faster tags identification. ECWAD is applicable for both single and dual antenna RFID tags. ECWAD overcomes the effect of the tag's rectifier capacitance on the detection delay and provide robust cutoff detection regardless of the input power level. ECWAD is evaluated under standardized timing parameters and identification protocols and compared to the existing CWAD. ECWAD not only increases the efficiency of identification protocol, it also provides a superior power saving of more than one order of magnitude.

Acknowledgment

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